A 40-bit Microprocessor for Logic Programming Language

Hideki ANDO, Hirohisa MACHIDA, Hiroshi NAKASHIMA,
and Masao NAKAYA

Mitsubishi Electric Corporation
4-1 Mizuhara, Itami, Hyogo, 664 Japan

1.Introduction

Parallel inference machine (*PIM*) systems are being developed in the Japanese fifth generation computer systems project. The PIM/m processes a Prolog-like parallel logic programming language, *FGHC* (flat guarded horn clauses), with two-dimensionally arrayed processor elements. The processor element has a processing unit (*PU*), a cache unit (*CU*), a main memory, a floating point processor unit and a network control unit as shown in Figure 1.

The PU chip is a 40-bit microprocessor for the execution of the logic programming language, under the control of microprogram stored in 64-bit by 64-Kword writable control store. It will operate at 16.7MHz clock and achieve high performance of 1.28MLIPS (logical inference per second) in "*append*".

2.Architecture

The PU chip comprises five pipeline stages: an instruction decode (*D-stage*); an operand address calculation (*A-stage*); an operand data fetch (*R-stage*); a dispatch of microinstruction (*S-stage*); and an execution (*E-stage*) as shown in Figure 2. In the D-stage, an instruction provided by an instruction cache in the CU is decoded with a 54-bit by 512-word operation decode table (*OPT*). In the A-stage, a calculation of an operand address and an instruction fetch are performed. The A-stage has copies of a 40-bit by 32-word register file (*RF*) and a few special registers for FGHC execution in the E-stage, which are used for the calculation of the operand address. In the D-stage, an operand at the calculated address is read. In the S-stage, dispatch of microinstruction, setup of operands and dereference are performed. The dispatch address is determined by the instruction and a tag of the operand. Special hardware of the dereference is implemented. Data is read repeatedly until the tag of read data is not "*a pointer*". In the E-stage, the instruction is executed by microprogram control. Main resources are a 32-bit ALU, a 40-bit by 32-word register file (RF), a 40-bit by 32-word work register (*WR*), an 8-bit by 512-word tag dispatch table (*TGT*) and a 16-bit by 32-word microprogram address stack (*MSTK*).

3.Layout Design

Figure 3 is a plot of the PU chip. The chip consists of 13K standard cells and eight macro cells such as RAMs and PLAs. The macro cells are automatically generated by module generators.

Two phase clocks are distributed as shown in Figure 4 to minimize clock skew. The clocks are driven by two stage buffers. A first buffer is placed at the upper side of the chip and drives second buffers. The second buffers are placed at right and left sides and drive all loads. Both outputs are connected in horizontal channels of a standard cell area. The width of the vertical lines is wide to reduce the resistance and the horizontal lines have minimum width to reduce load capacitance. Less than 1ns skew to control gates of flip-flops was confirmed by simulation. From the view point of the automatic layout, this method has the advantage over a hierarchical and tree clock distribution method[1][2]. Because it is necessary to control load balance for each buffer, control line length and adjust the buffer size if necessary after the layout on a hierarchical clock distribution method, but they are difficult for a commercial automatic place and route program.

The device features are summarized in Table 1. The chip is being fabricated in a 0.8μm double-metal CMOS technology. A total of 384K transistors are integrated in a 16.3 x 13.6mm die.

4.Conclusion

A 40-bit microprocessor for logic programming language has been designed. The layout was completed using standard cells and macro cells generated by module generators. The clock skew was minimized by locating two drivers on opposite sides of the chip. The chip will operate at 16.7MHz clock and achieve high performance of 1.28MLIPS in "*append*".

5.Acknowledgment

The authors would like to thank Dr. H. Komiya, Dr. T. Nakano and Dr. Y. Horiba for their encouragement, and also thank Dr. S. Uchida and researchers in the ICOT fourth laboratory.

6.Reference
[1] T. Tokumaru, F. Masuda, C. Hori, K. Usami, M. Miyata and J. Iwamura, "Design of a 32bit microprocessor, TXI", in Symp. VLSI Circuits Dig. Tech. Papers, Aug. 1988, pp.33-34.

[2] S. Boon, S. Butler, R. Byrne and B. Setering, "High performance clock distribution for CMOS ASICS", in Proc. Custom Integrated Circuits Conf. May 1989, pp.15.4.1-15.4.5.

Table 1 Device Features

Data width	40bit
ALU	32bit
Operation decode table	54bit x 512word
Register file	40bit x 32word x 2
Work register	40bit x 32word
Tag dispatch table	8bit x 512word
Microprogram address stack	16bit x 32word
Transistor count	384K
Chip size	16.3 x 13.6 mm
Package	361 pin PGA
Clock	16.7MHz
Power supply	5V
Process technology	0.8μm double-metal CMOS

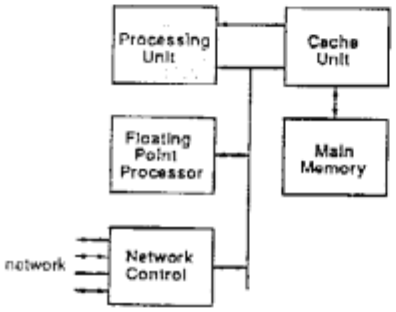

Figure 1 System Configulation of the Processor Element of the PIM

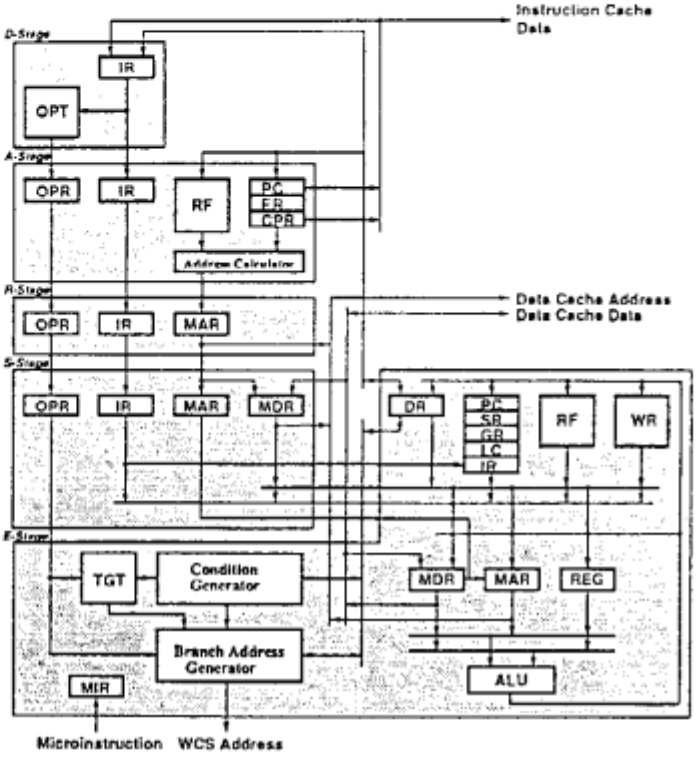

Figure 2 Architecture

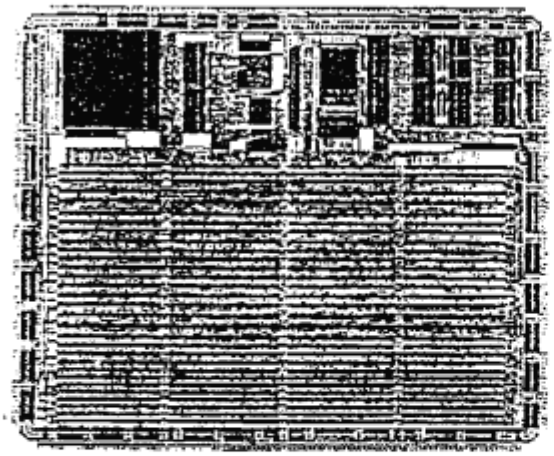

Figure 3 Chip Plot

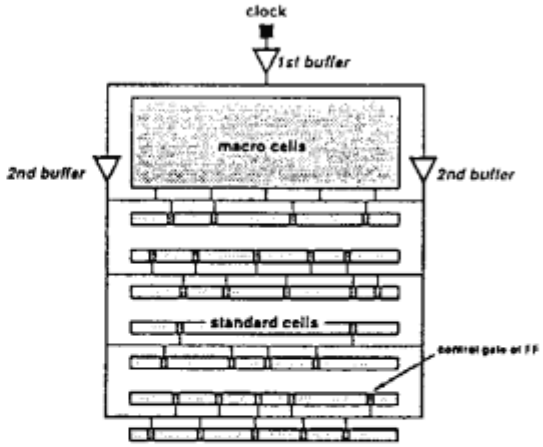

Figure 4 Schematic Diagram of Clock Distribution