ICOT Technical Memorandum: TM-0386

TM-0386

Inference Machines in FGCS Project
(Hardcopy of the Slides)

by
S. Uchida

September, 1987

ICOT
Mita Kokusai Bldg. 21F
4-28 Mita 1-Chome
Minato-ku Tokyo 108 Japan

(03) 456-3191~5
Telex ICOT J32964

Institute for New Generation Computer Technology

Inference Machines in FGCS Project

Shunichi Uchida

ICOT

Goal of FGCS project

R & D of basic technology for

KIPS (Knowledge Info. Processing Sys.)

Kernel of KIPS

Central Mechanism:

Logical Inference using Knowledge Base

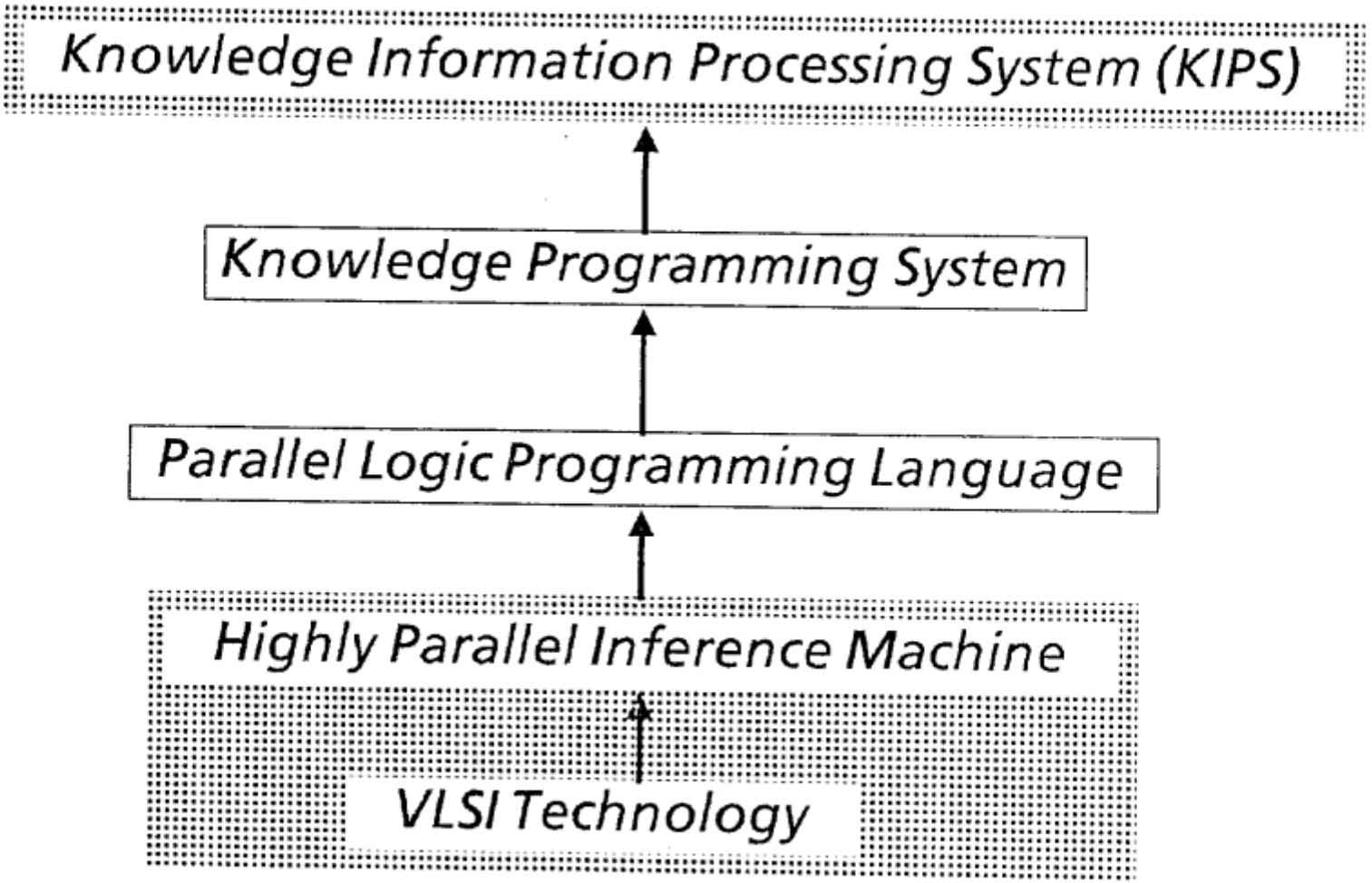
Kernel Lang. (KL)

⇒ Logic Programming

Machines ⇒ Inference Machines

PIM, SIM

Basic Software System



R & D of Inference Machines

1. Sequential Inference Machine (SIM)

H/W: PSI(I,II), CHI(I,II)

Lang: KL0, ESP(Object-oriented Prolog)

S/W: SIMPOS

2. Parallel Inference Machine (PIM)

H/W: PIM(I,II), Multi-PSI

Lang: KL1(Based on GHC)

S/W: PIMOS, PIMPOS

Project's Span = 10 Years

1. Initial Stage (1982 – 1984)
   - Element technology of PIM
   - KL1 design
   - PSI-I, CHI-I, SIMPOS
2. Intermediate Stage (1985 – 1988)
   - PIM-I: 100 PE, 10 – 20M LIPS
   - Multi-PSI: 64 PE
   - PIMOS, KL1(B, C, P, U)
3. Final Stage (1989 – 1991)
   - PIM-II: 1000 PE, 100M – 1G LIPS
   - PIMPOS, KL2

Sequential Inference Machine (SIM)

Software development tool for FGCS

PSI: Personal Workstation

PSI-I : 30K (Ave.), 35K (Append)

PSI-II : 150K (Ave.), 333K (Append)

CHI: Backend-type Prolog Machine

CHI-I : 280K (Append)

CHI-II : 490K (Append)

Software system:

KL0 and ESP (PSI)

SIMPOS: Multi-window based Personal OS

PSI: Personal SIM

1. Outline

- Logic programming work station
- Common standard tool for the project
- Multi-window based interface
- 30 KLIPS and 80 MB main mem.(PSI-I)
- LAN and DDX-network connection

2. Language and Software

- KL0 = Prolog level (Extended)
- ESP = System description lang.
  KL0 + Object-oriented features
- SIMPOS: Personal OS written in ESP
  2100 class modules / 375K lines

Main features of PSI-I and PSI-II

	PSI-I	PSI-II
Device	TTL (Fast)	CMOS-G.A., TTL
Cycle time	200 ns	200 ns
Word width	40 bits	40 bits
WCS	64b x 16KW	53b x 16KW
Cache memory	4KW x 2	4KW x 1
Main memory	16MW (Max)	64MW (Max)
Memory chip	256 Kbit	1 Mbit
Max. No. of Process	64	S/W defined
Machine code	Table type	WAM type
Structure data	Sharing	Copying
Exe. speed(Average)	30 KLIPS	150 KLIPS
Exe. speed(Append)	35 KLIPS	333 KLIPS

Performace of PSI-I and PSI-II

	PSI-I (KLIPS)	PSI-II (KLIPS)
Append	35	333
Naive Reverse	34	271
Quick Sort	40	132
Tree Traverse	41	100
8 Queens	60	162

CHI: Cooperative High-speed IM

- Backend-type Prolog machine
- Connected to PSI or UNIX based workstation
- Experimental development of fastest possible machine
- WAM type machine instruction set

Main features of CHI-I and CHI-II

	CHI-I	CHI-II
Device	CML	CMOS-G.A., TTL
Cycle time	100 ns	170 ns
Word width	32 bits	40 bits
WCS	78b x 16KW	same
Cache memory	16KW x 2	same
Main memory	64MW (Max)	128MW (Max)
Memory chip	256 Kbit	1 Mbit
Machine code	WAM type	extended WAM
Structure data	Copying	same
Exe. speed(Append)	280 KLIPS	490 KLIPS

SIMPOS: SIM Prog. & Operating Sys.

- Efficient programming environment for ESP (Extended-Self contained Prolog)
  ⇒ System and Knowledge description
- SIMPOS modules are fully organized based on object-oriented model.
  ⇒ System classes are open for users by inheritance mechanism.
- Multi-window based interactive man-machine interface
- Distributed OS functions for LAN and DDX-network
- Japanese character I/O is a standard function.

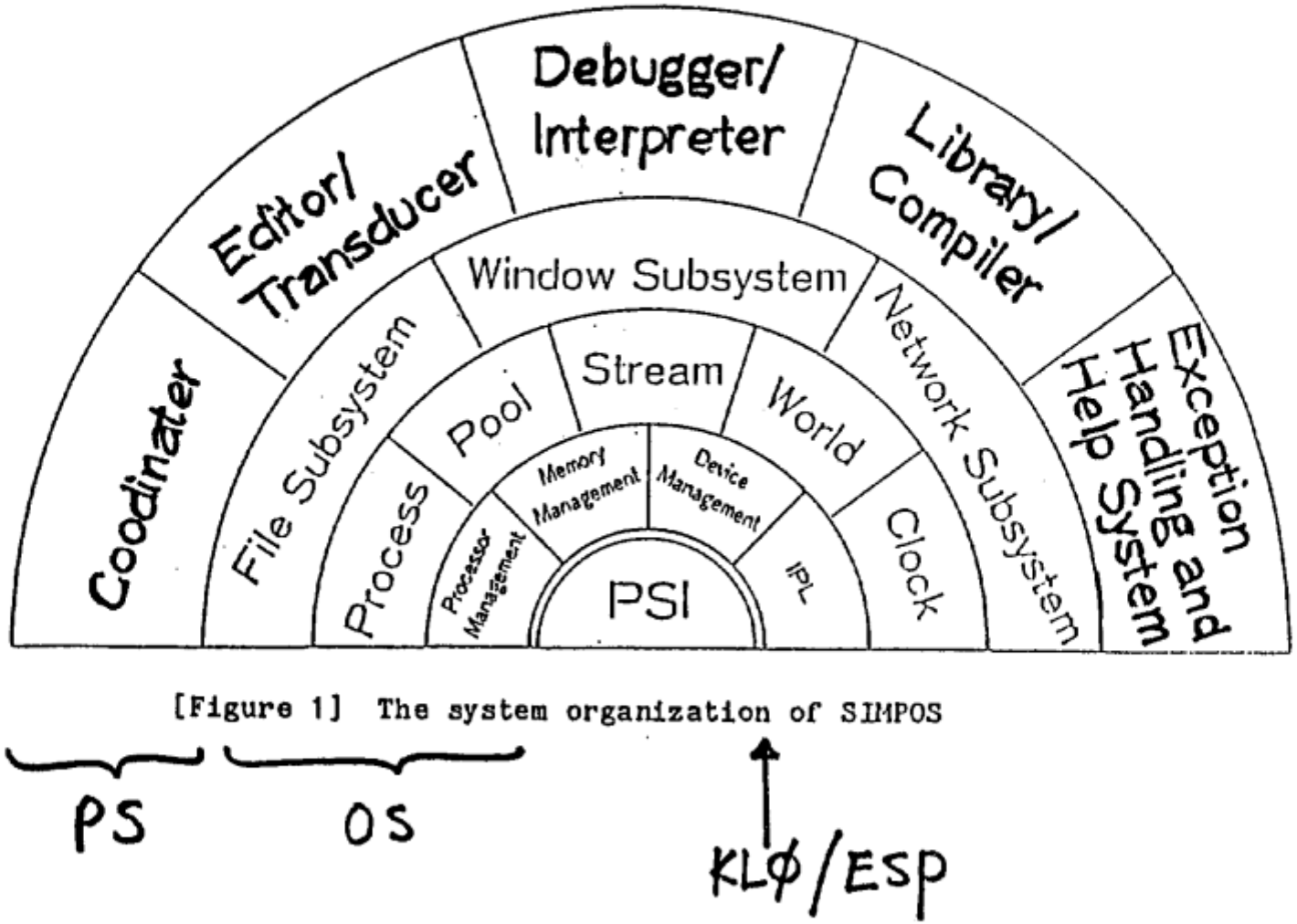
ESP: Extended-self contained Prolog

- ESP = KL0

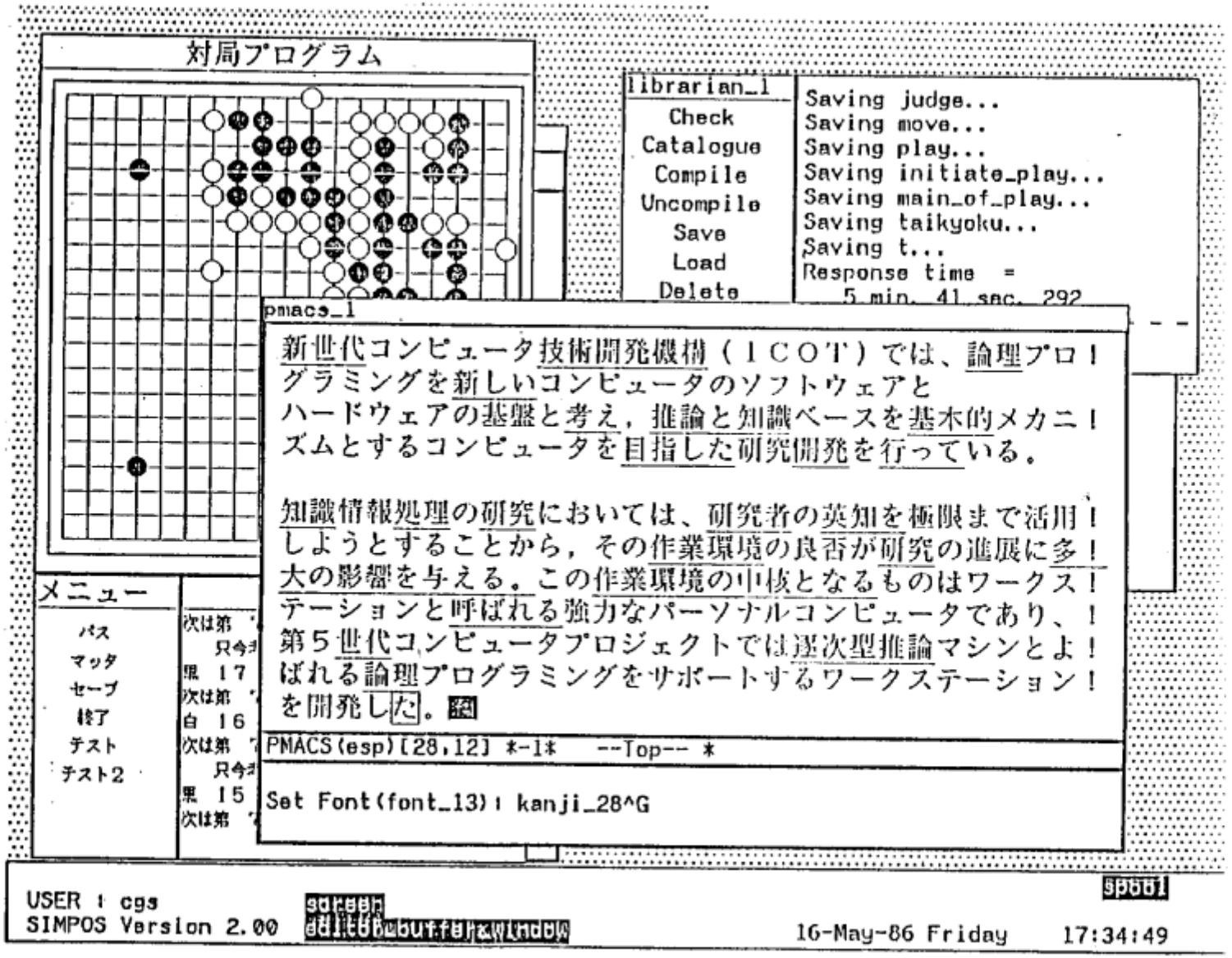
  + Object-oriented modularization

  + Macro processor

- Used for SIMPOS description
- Used for Knowledge description
- Firmware support is made on PSI



[Figure 1] The system organization of SIMPOS


対局プログラム
librarian_1
Check
Catalogue
Compile
Uncompile
Save
Load
Delete
Saving judge...
Saving move...
Saving play...
Saving initiate_play...
Saving main_of_play...
Saving taikyoku...
Saving t...
Response time =
5 min. 41 sec. 292
pmacs_1
新世代コンピュータ技術開発機構（ＩＣＯＴ）では、論理プログラミングを新しいコンピュータのソフトウェアとハードウェアの基盤と考え，推論と知識ベースを基本的メカニズムとするコンピュータを目指した研究開発を行っている。
知識情報処理の研究においては、研究者の英知を極限まで活用しようとすることから，その作業環境の良否が研究の進展に多大の影響を与える。この作業環境の中核となるものはワークステーションと呼ばれる強力なパーソナルコンピュータであり、第５世代コンピュータプロジェクトでは逐次型推論マシンとよばれる論理プログラミングをサポートするワークステーションを開発した。
PMACS(esp)[28,12] *-1* --Top-- *
Set Font(font_13)↓ kanji_28^G
メニュー
パス
マッタ
セーブ
終了
テスト
テスト2
次は第
只今
黒 17
次は第
白 16
次は第
只今
黒 15
次は第
USER : cgs
SIMPOS Version 2.00
16-May-86 Friday 17:34:49

PIM-I: Intermediate Stage Target

1. Scale of experimental H/W

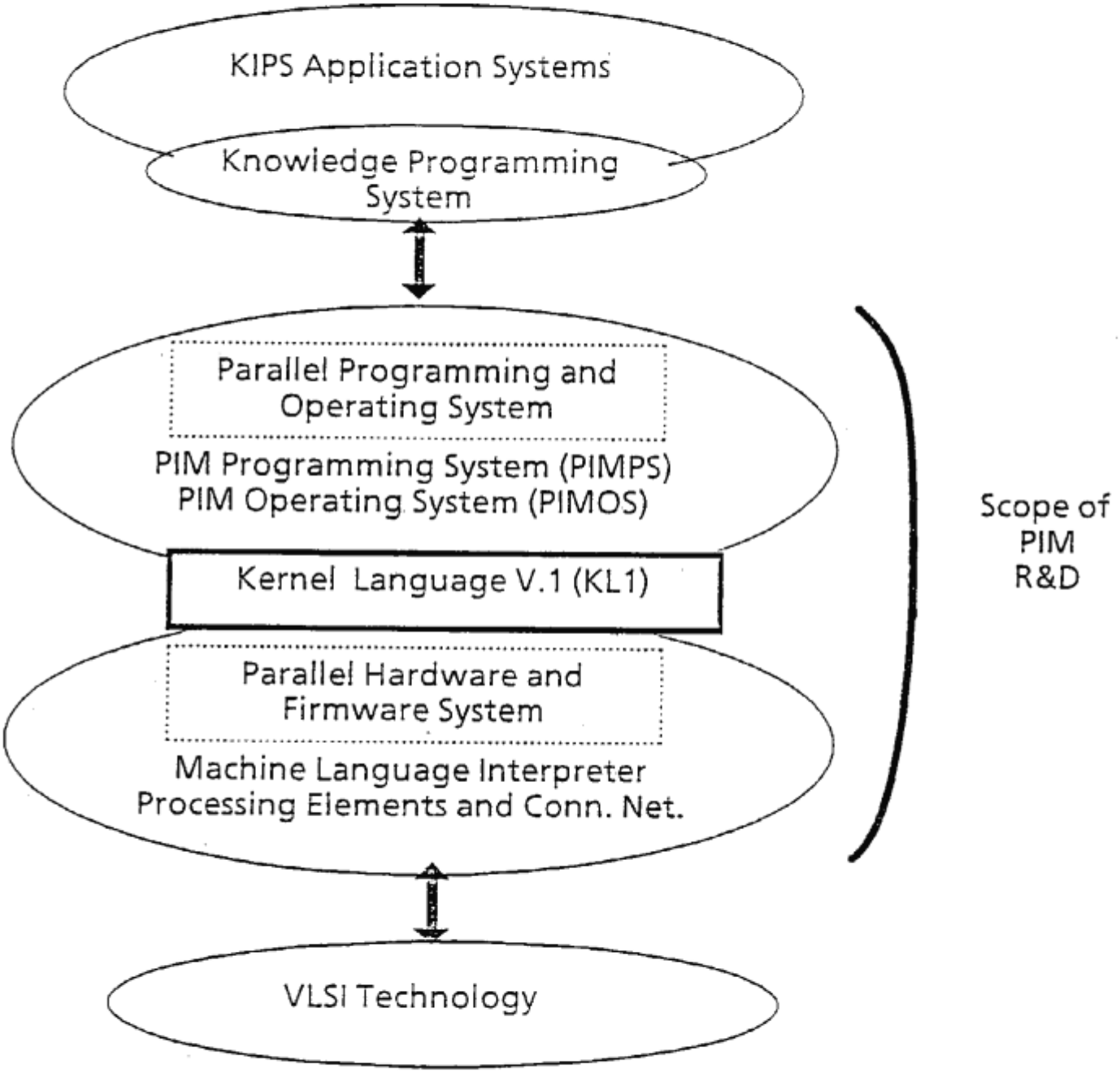
   No. of PE = 100

2. Processing-speed = 10 - 20M LIPS/System

3. Machine lang. = KL1 based on GHC

4. Supporting PIMOS and stable H/W

Scope of PIM R&D



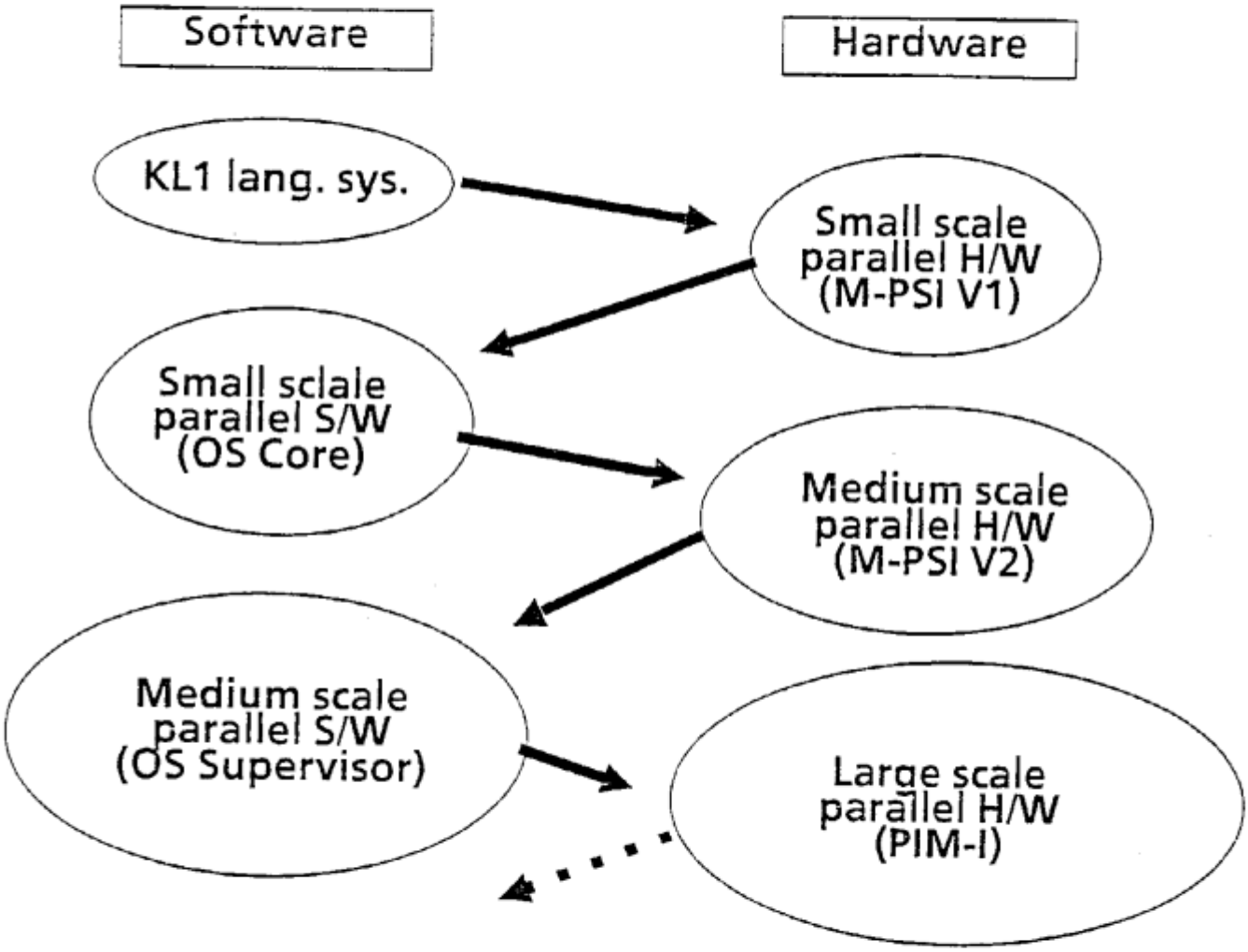
An approach to PIM-I and PIMOS

1. Organizing systematic parallel S/W development and coupling it with parallel H/W development
2. Step-by-step (Bootstrapping) approach for H/W and S/W development using Multi-PSI system

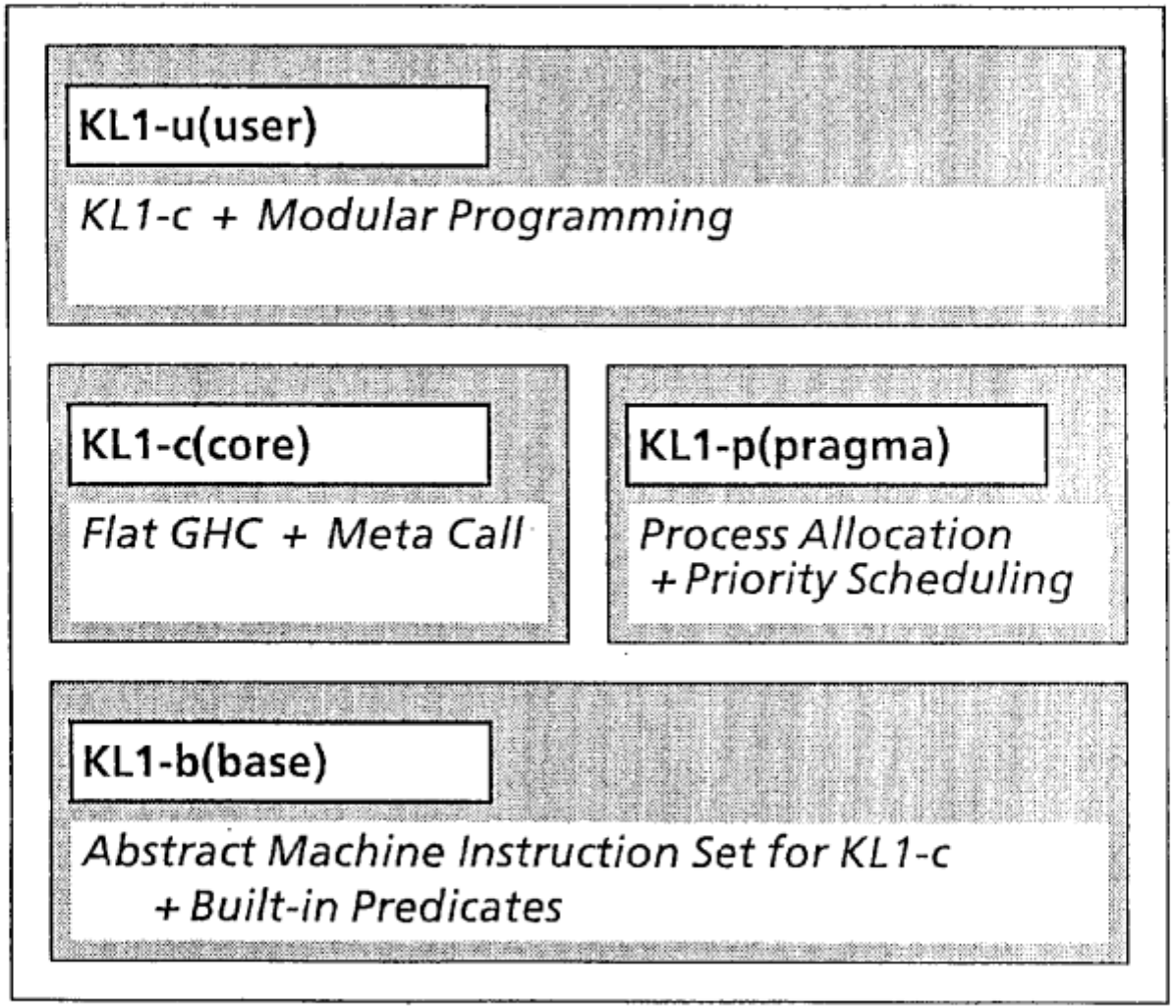
How to Proceed Parallel S/W R&D

Basic idea = Bootstrapping

Small to Large, Step by step



KL1 Language System



KL1 language features

1. **KL1-C** Core of KL1 := GHC

   - Committed-choice AND parallel language
   - Very simple, suitable for F/W, H/W implementation.
   - Logic programming formalism is maintained.
   - Concepts realized:

     Data-driven/demand-driven computations,

     Non-strict data structures,

     Dynamic process/data structures,

     Object-oriented programming, etc

2. **KL1-B** Base of KL1: Machine language

- Abstract machine inst. set using registers
- Compiler optimization is introduced:

  Clause indexing, Perpetual process (TRO)

  etc
- Extension for PE-PE, cluster-cluster

  communication
- Passive unify (wait, read),

  Argument arrangement (put, set, write),

  Active unify (get),

  Exec. Control (enqueue_goal, proceed),

  Built-in predicates
- Incremental GC support (MRB)

3. **KL1-P** Pragma of KL1: Notation for job and resource control

- Specifying the way of dividing a job into several pieces of parallel processable subjobs.
- Specifying the amount of computing resources to the subjobs.

4. **KL1-U** User lang. of KL1: System description language

- Parallel object-oriented language
- Based on message passing model
- Modularization based on class and inheritance
- A KL1-U program is compiled into KL1-C

Configuration of PIM-I

1. Hierarchical structure – Cluster
    - Inter-cluster: Packet switching net
    - In cluster: Parallel cache and shared memory
2. Cluster structure
    - 1.5 - 3M LIPS/Cluster
    - 8 PEs and 1 shared-memory
    - Communication support H/W

3. Tag-architecture based PE

- 200 - 500K LIPS/PE
- Machine lang: KL1-B (Compiler optimization is considered)
- 40 bit word (8 bit tag)
- Process switching support
- Real-time GC support (MRB)
- 1 PE/PCB by VLSIs

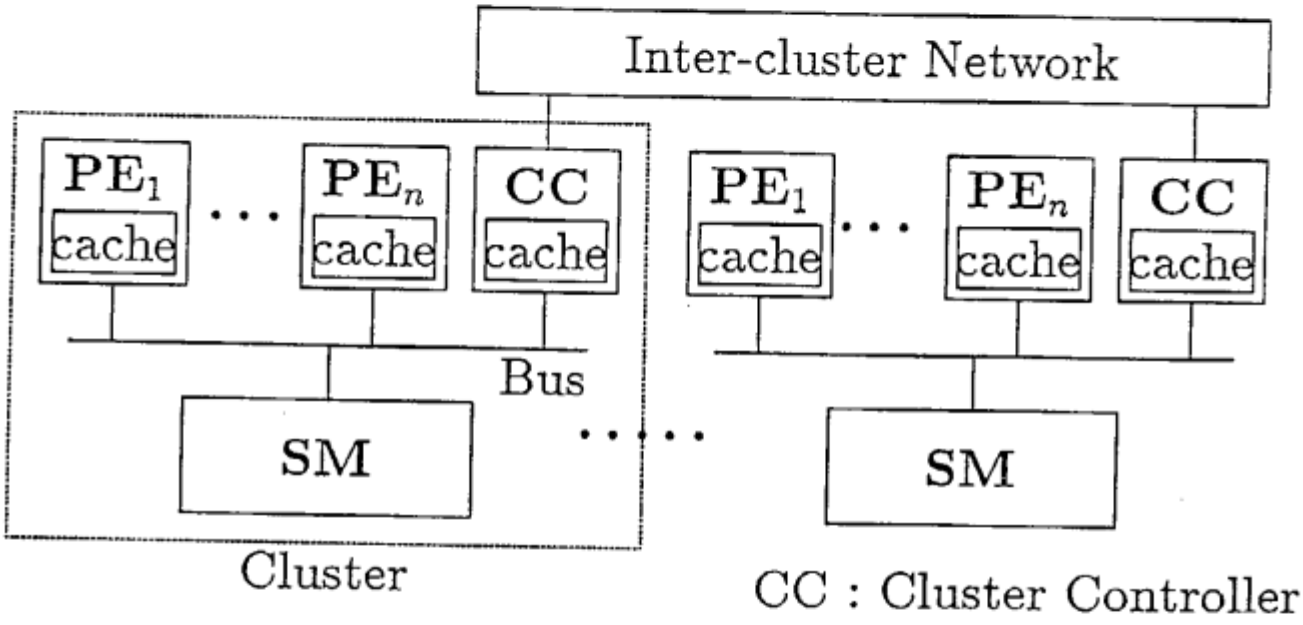


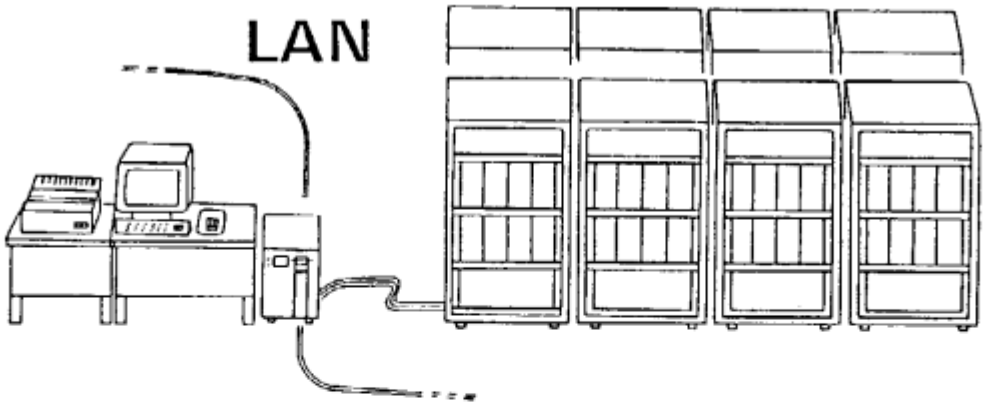
Figure 1: PIM Overview

Important features of PIMOS

- Self-contained OS written in KL1-U
- Static and dynamic job allocation
- Based on object-oriented model
  (Stream-based communication)
- Built on Multi-PSI system and moved to PIM-I
- Cross programming environment on PSI-II

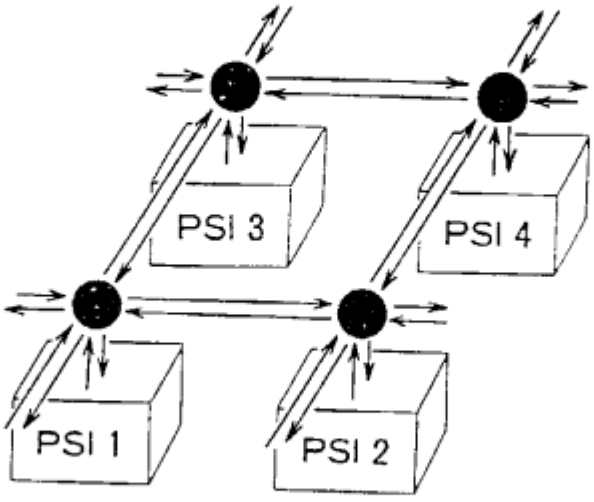
Multi-PSI System: Version 2 (1988)

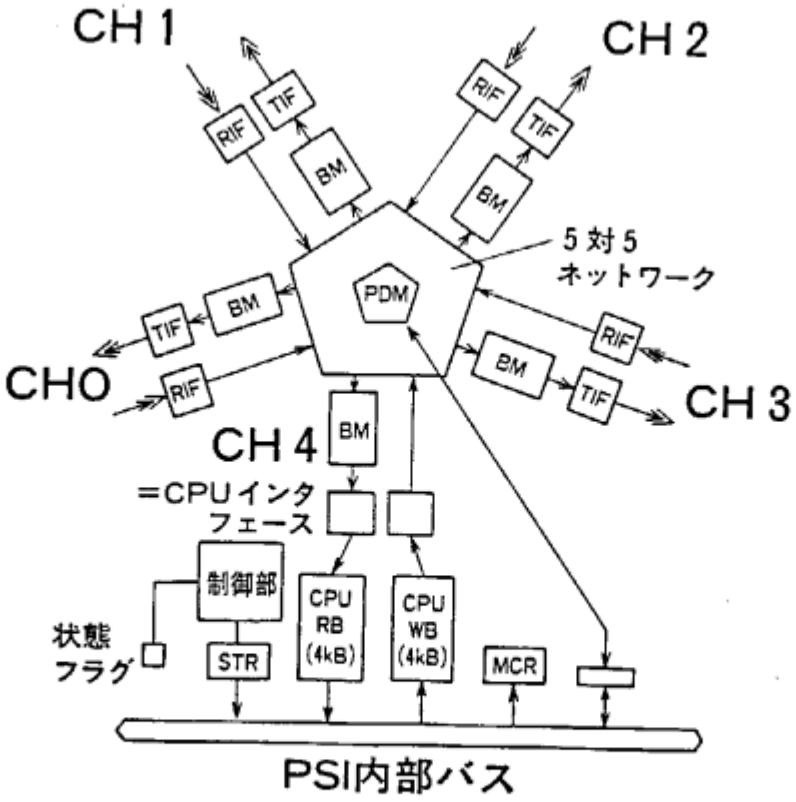
- 8 to 64 PEs (8 PEs/Cabinet)
- KL1-B interpreter: Firmware implemented
  (100 - 150K LIPS/PE for KL1-B)
- Front-end: PSI-II (KL0 and KL1)



Multi-PSI System: Network hardware

- Two-dimensional mesh network
- 5 channels/node, I/O FIFO buffers/channel
- 2 independent byte-busses/chann.
  for input and output
- Packet routing logic (using 2 LSI's)
- Max. transfer rate 5 MB/sec


PSI 3
PSI 4
PSI 1
PSI 2


CH 1
CH 2
RIF
TIF
BM
5 対 5
ネットワーク
PDM
CHO
CH 3
CH 4
=CPUインタ
フェース
制御部
状態
フラグ
STR
CPU
RB
(4kB)
CPU
WB
(4kB)
MCR
PSI内部バス

Intermediate Stage Plan